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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,495	02/11/2002	William A. Stevens, JR.	042390.P9143	6012

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 09/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/073,495	STEVENS, ET AL.
	Examiner	Art Unit
	Tse Chen	2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05212002,01202004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on May 21, 2002 and January 20, 2004, were filed before the mailing date of the first Office Action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

2. Claims 8, 25 and 34 are objected to because of the following informalities:

- As per claim 8, the sentence "...import table to store GUIDs of the set of modules..." is awkward and should be changed to "...import table stores GUIDs of the set of modules..." or the like.
- As per claim 25, the semicolon at the end of "...the BIOS further including" on line 12 should be a colon.
- As per claim 34, the sentence "...core to select for execution..." on line 20 is awkward and should be changed to "...core selects for execution..." or the like.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens, U.S. Patent 6633976, in view of Patel, U.S. Patent 5999989.

5. In re claim 1, Stevens discloses a method comprising:

- Starting execution of a basic input output system (BIOS) [col.2, ll.14-29], the BIOS having a plurality of modules [fig.2; col.2, l.56 – col.3, l.15].
- Scheduling execution of modules of the plurality of modules [col.3, ll.1-15; sequentially schedules modules for execution].
- Dispatching the scheduled modules for execution [col.3, ll.1-31].

6. Stevens did not disclose explicitly the determining of resources required by the plurality of modules.

7. Patel discloses a method comprising:

- Determining resources required by a plurality of modules [devices] [col.4, ll.31-44].

8. It would have been obvious to one of ordinary skill in the art, having the teachings of Stevens and Patel before him at the time the invention was made, to modify the system of Stevens to include the teachings of Patel, in order to enhance the robustness of the BIOS [Patel: col.1, ll.51-56]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to enhance the robustness of the BIOS.

9. As to claim 2, Patel discloses initializing a memory [register set] of the platform after the scheduled modules are dispatched [col.6, l.10 – col.7, l.42].

10. As to claim 3, Stevens discloses calling a module [requested BIOS module] of the plurality of modules for execution during execution of another module [dispatch manager] of the plurality of modules [col.5, ll.37-52].

11. As to claim 4, Patel discloses the method wherein calling a module of the plurality of modules further comprises:

- Saving a return address [col.7, ll.43-47; far return to POST].
- Determining a physical address [pointer in location] of the module [col.7, ll.1-29].
- Executing an instruction stored at the physical address of the module [col.7, ll.11-29].
- Executing an instruction [performs device specific write-protection] stored at the saved return address when the module execution is complete [col.7, ll.43-47].

12. As to claim 5, Patel discloses the method wherein determining the physical address of the module comprises looking up the physical address [pointer] in an import table [part of ROM header data structure] of the other module [col.7, l.1 – col.8, l.46].

13. As to claim 6, Patel discloses the method wherein a module of the plurality of modules comprises [fig.1a]:

- A globally unique identifier (GUID) [72 bit serial id] to identify the module [col.7, ll.48-59].
- A resource list [part of ROM header data structure] to store information identifying resources needed by the module to operate [col.7, ll.1-10].
- An import table [part of ROM header data structure] to store physical addresses [pointers 166, 182] of a set of modules [init, boot code] of the plurality of modules that the module may call during execution [col.7, ll.1-42; col.8, ll.6-46].
- A service that when executed performs a predetermined function [col.3, l.58 – col.4, l.10].

- An export table [interrupt table] to store a value [register argument] corresponding to a physical address of the service [col.7, ll.11-29; col.8, ll.6-46].
- An interface [via handle id] operatively coupled to the GUID, resource list, the service, the import table, and the export table, wherein the interface is addressable by a calling agent [POST] via the GUID to provide the calling agent access to the resource list, the service, the import table, and the export table [col.3, l.58- col.4, l.10].

14. As to claim 7, Patel discloses the method wherein the value [DI] stored by the export table is an offset from a start address of the module [col.8, ll.26-33].

15. As to claim 8. Patel discloses the method wherein the import table [allocation map] stores GUIDs [handle ids] of the set of modules of the plurality of modules [col.3, l.58 col.4, l.10; relative to POST module].

16. As to claim 9, Patel discloses the method comprising:

- Starting execution of a first module [POST] of the plurality of modules [col.4, l.46 – col.5, l.57]. Determining whether the first module is chainable with another module [initialization of other devices] of the plurality of modules [col.7, ll.11-47; col.14, ll.13-26; POST makes call and returns as in a chain].
- Determining whether a hardware component [actual device] associated with the first module is present in the platform if the first module is chainable [col.6, ll.10-47].
- Completing execution of the first module if the hardware component associated with the first module is present in the platform [col.6, ll.10-47; device is activated in step 220].
- Starting execution of a second module of the plurality of modules without completing execution of the first module if the hardware component associated with the first module

is not present in the platform [fig.2; col.6, ll.10-47; if device is not present, steps 206-208 are repeated with first device taken out of allocation map and second device being executed instead].

17. As to claim 10, Patel discloses the method wherein the first module includes a data structure [allocation map] to store a physical address of the second module [col.3, l.58 – col.4, l.10].

18. As to claim 11, Patel discloses each and every limitation of the claim as discussed above in reference to claim 9. Furthermore, Patel discloses multiple modules [devices] that can be chained by one with ordinary skill in the art [fig.5c].

19. As to claim 12, Stevens discloses the method wherein completing execution of the second module [task associated with module] further comprises returning to a calling agent [dispatch manager] that called the first module [col.9, ll.16-36; dispatch manager sequentially executes list of tasks with each task returning to the dispatch manager before executing next task].

20. As to claim 13, Stevens discloses the method comprising:

- Executing a call made by a calling agent [dispatch manager] to a first module of the plurality of modules, wherein the call [task] is one of a set of calls, each call of the set of calls being associated with a module of a set of modules of the plurality of modules, the associations being dependent on a configuration of the platform [col.3, ll.1-31; col.5, ll.37-52; modules required for operation].
- Starting execution of the first module of the plurality of modules in response to the call [col.3, ll.1-31; col.5, ll.37-52].

- Determining which module of the set of modules is associated with the call [col.5, ll.45-52].
- Starting execution of the module associated with the call [col.3, ll.1-31; col.5, ll.37-52].

21. As to claim 14, Stevens discloses the method comprising returning to the calling agent [dispatch manager] when execution of the module associated with the call is complete [col.9, ll.16-36; dispatch manager sequentially executes list of tasks with each task returning to the dispatch manager before executing next task].

22. As to claims 15-24, Stevens and Patel disclose each and every limitation of the claims as discussed above in reference to claims 1-14. In particular, Patel discloses a machine readable medium [firmware] containing instructions that when executed by a machine [fig.1; computer system], causes the machine to perform operations comprising the method of claim 1 [col.3, ll.40-48; col.4, ll.11-44].

23. In re claim 15, each and every limitation of the claim is disclosed as discussed in reference to claim 1.

24. In re claim 16, each and every limitation of the claim is disclosed as discussed in reference to claim 2.

25. In re claim 17, each and every limitation of the claim is disclosed as discussed in reference to claim 3.

26. In re claim 18, each and every limitation of the claim is disclosed as discussed in reference to claim 4.

27. In re claim 19, each and every limitation of the claim is disclosed as discussed in reference to claim 6.

28. In re claim 20, each and every limitation of the claim is disclosed as discussed in reference to claim 9.

29. In re claim 21, each and every limitation of the claim is disclosed as discussed in reference to claim 11.

30. In re claim 22, each and every limitation of the claim is disclosed as discussed in reference to claim 12.

31. In re claim 23, each and every limitation of the claim is disclosed as discussed in reference to claim 13.

32. In re claim 24, each and every limitation of the claim is disclosed as discussed in reference to claim 14.

33. As to claims 25-33, Stevens and Patel disclose each and every limitation of the claims as discussed above in reference to claims 1-14. In particular, Stevens discloses a system [computer 10a], comprising:

- A plurality of hardware components [col.5, ll.1-26, l.54 – col.6, l.2].
- A first memory device [system memory 13] to store a BIOS, the BIOS having a plurality of modules [fig.2; col.5, ll.27-52].
- A processor [CPU 11] coupled to the plurality of hardware components [via PCI bus 14] and the first memory device [col.5, ll.1-26].

34. In re claim 25, each and every limitation of the claim is disclosed as discussed in reference to claim 1.

35. In re claim 26, each and every limitation of the claim is disclosed as discussed in reference to claim 2.

36. In re claim 27, each and every limitation of the claim is disclosed as discussed in reference to claim 3.

37. In re claim 28, each and every limitation of the claim is disclosed as discussed in reference to claim 4.

38. In re claim 29, each and every limitation of the claim is disclosed as discussed in reference to claim 6.

39. In re claim 30, each and every limitation of the claim is disclosed as discussed in reference to claim 9.

40. In re claim 31, each and every limitation of the claim is disclosed as discussed in reference to claim 11.

41. In re claim 32, each and every limitation of the claim is disclosed as discussed in reference to claim 12.

42. In re claim 33, each and every limitation of the claim is disclosed as discussed in reference to claim 13.

43. As to claims 34 –41, Stevens and Patel disclose each and every limitation of the claim as discussed above in reference to claims 1-14 and 25. In particular, Stevens discloses the BIOS comprising:

- A core [dispatch manager] operatively coupled to the plurality of modules, wherein the core selects for execution a set of module from the plurality of modules [col.5, ll.27-53].

44. In re claim 34, each and every limitation of the claim is disclosed as discussed in reference to claims 1 and 25.

45. In re claim 35, each and every limitation of the claim is disclosed as discussed in reference to claims 1, 3 and 25.

46. In re claim 36, each and every limitation of the claim is disclosed as discussed in reference to claims 1, 4, 5, and 25.

47. In re claim 37, each and every limitation of the claim is disclosed as discussed in reference to claims 1, 6 and 25.

48. In re claim 38, each and every limitation of the claim is disclosed as discussed in reference to claims 1, 6 and 25.

49. In re claim 39, each and every limitation of the claim is disclosed as discussed in reference to claims 1, 9 and 25.

50. In re claim 40, each and every limitation of the claim is disclosed as discussed in reference to claims 1, 9 and 25.

51. In re claim 41, each and every limitation of the claim is disclosed as discussed in reference to claims 1, 11 and 25.

Conclusion

52. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited U.S. patent documents describes various systems with multiple modules chainable for specific configuration.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
September 13, 2004

REHANA PERVEEN
PRIMARY EXAMINER